An implementation of level set based topology optimization using GPU

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ABSTRACT

This work presents the implementation of a topology optimization method based on level set method in massively parallel computer architectures, in particular on Graphics Processing Units (GPUs). Such architectures are becoming so popular during last years for complex and tedious scientific computation. They are composed of dozens, hundreds, or even thousands of cores specially designed for parallel computing. The speedup process consists of using these graphic units to exploit data parallelism of expensive and parallelizable parts of the method, while non-parallelizable parts are calculated in standard processing units (CPUs). The aim is to avoid data transfer delays between GPU and CPU memories. The paper analyses the computational complexity of the different steps of the method. On the one side, the parallelization of finite element method is discussed, including stiffness assembly and different solvers on the GPUs. On the other side, the parallelization of specific operations for the level set method is also analyzed, including shape and topology sensitivity analyses. The implementation of the method is benchmarked with several tests. In these tests, the massively parallel results are compared with the sequential version of the method. The results show the advantages and disadvantages of the implementation of this method using massively parallel computer architecture.